Seeding of Silicon Wire Growth by Out-Diffused Metal Precipitates

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We propose the out-diffused metal precipitates (OMP) method to seed metal catalysts for bottom-up silicon wire growth. We first in-diffuse the silicon substrate with a fast-diffusing metal (e.g., copper), and then anneal with a temperature profile tuned to out-diffuse the metal to favorable nucleation sites on the surface. Vapor–liquid–solid (VLS) silicon wire growth on seeds from the OMP method is demonstrated. The OMP method has the potential to seed wires of any size at any position on a three-dimensional surface, in a high-throughput manner.

Silicon nanowires and microwires have potential for applications in integrated circuits,[1] solar cells,[2–5] lithium batteries,[6] and biological sensors.[7] For example, Kelzenberg et al.[4] have demonstrated enhanced light absorption and decreased materials usage in solar cells fabricated from silicon microwire arrays, with distinct performance advantages over nanowire-based solar cells. A common bottom-up approach to synthesizing silicon wires is the VLS method, in which liquid metal droplets are used to catalyze crystalline wire growth. In the VLS method, first proposed by Wagner,[8] a metal catalyst is seeded onto the surface of a silicon substrate, and nanowires are grown by chemical vapor deposition (CVD) with a gas such as silane or silicon tetrachloride. The metal catalyst generally used is gold;[9] however other metals such as copper[10–15] have been utilized successfully.

Many techniques have been demonstrated for seeding metal catalysts on silicon substrates. A standard method is to deposit a thin metal layer, typically nanometers thick, and heat the substrate until the film dewets into droplets. However, on a smooth surface the positions of these droplets are random, and film thickness gives only limited control over wire diameters.[16] To gain control over position of the droplets, an ordered array of pits on the substrate can be created with a combination of photolithography and potassium hydroxide etching (e.g., on a <100> silicon substrate). The periodic curvature of the metal film guides the dewetting of the layer.[16] Photolithography can also be used with a lift-off procedure to pattern the metal catalyst. This has been demonstrated by Choi et al.[17] with gold droplets patterned into potassium hydroxide etched pits, and by Kayes et al.[18] with gold and copper islands separated by an oxide. For smaller feature sizes, nanoimprint or nanosphere lithography techniques are used. In nanoimprint lithography, e-beam lithography is used to create a stamp to pattern resist, and is followed by a lift-off procedure.[19] Nanosphere lithography, in which a metal (e.g., gold) is patterned by a layer of polystyrene nanospheres, has been shown to successfully create ordered arrays of nanowires in a hexagonal pattern with a gold catalyst.[20,21]

Other techniques for metal catalyst seeding include electrodeposition of gold into an anodized alumina[9,22] or other oxide template,[23] using block copolymers to pattern,[24] and gold ion implantation into a silicon substrate.[25] For large arrays of wires, a patterning method commonly used is the deposition of a commercial solution of nanosized gold colloids over the substrate. By first depositing a layer of poly-L-lysine, which is positively charged, the negatively charged colloids distribute evenly over the surface.[26,27] Nanoimprint lithography can be used to stamp the poly-L-lysine, obtaining further control over the distribution of colloids.[9]

These techniques for metal catalyst seeding provide varying levels of control on seed diameter and placement. In particular, in most of these techniques, the seed size is controlled by the patterning technique (e.g., with photolithography and potassium hydroxide etching, the size of the catalyst seeds are dependent on the dimensions of the etch pits).

In this contribution, we propose a new method for seeding metal catalysts for silicon wire growth. The OMP method has the potential for controlling seed diameter and placement in a high-throughput manner. A schematic of the major steps is shown in **Figure 1**. In the OMP method, the silicon substrate is intentionally contaminated at a high temperature with the metal catalyst, and quenched rapidly to prevent the metal impurity from diffusing out of the silicon bulk. The surface of the substrate can then be patterned to create surface defects that serve as favorable precipitation points, such that when the substrate undergoes a slow cooling from high temperature, the metal precipitates at these favorable locations. The details of the OMP method are described in depth in the Experimental Section.

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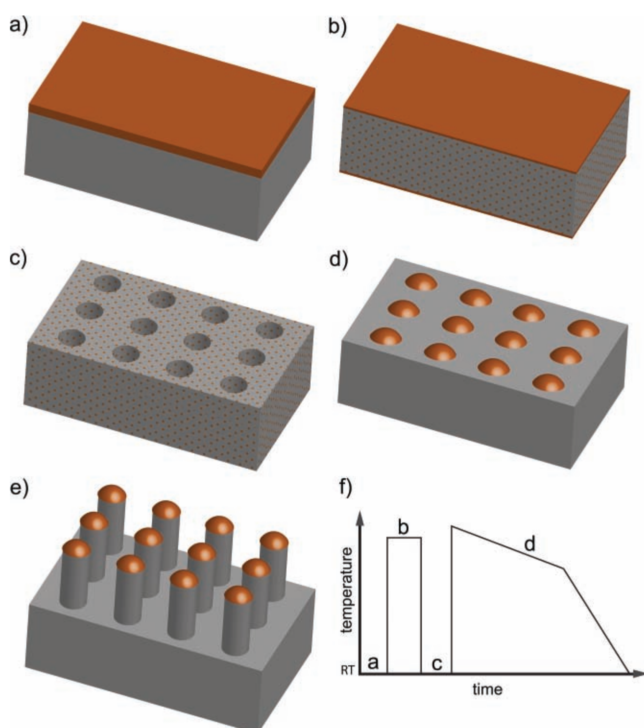

Figure 1. The steps in the OMP method are a) metal catalyst deposition, b) in-diffusion by high-temperature annealing, c) surface polishing and patterning, d) out-diffusion by slow-cooling, and e) wire growth. The relative time versus temperature is shown in (f).

The OMP method has the potential to control seed diameter by varying parameters such as the in-diffusion temperature of the metal. Thus, diameter control can be decoupled from the surface patterning technique used. The positions of the seeds can be controlled through the intentional creation of surface defects. Additionally, the OMP method is not sensitive to metal deposition thickness, making it conducive to low-cost applications. We believe the greatest advantage of the OMP method over existing methods is the potential to create controlled patterns of seeds on arbitrary three-dimensional surfaces in a high-throughput manner. In this communication, we show proof-of-concept of the OMP technique, using copper as the metal catalyst for VLS silicon wire growth.

As impurity kinetics plays a determining role in the OMP method, it is instructive to review the properties of metal point defects in silicon. **Figure 2** plots the solubility of several metals shown to be successful in catalyzing silicon wire growth in previous studies,[9,11,28] as a function of diffusivity in silicon for a temperature of 1200 °C. Copper has a high solubility and diffusivity at elevated temperatures, which allows it to be easily manipulated with the OMP method. Although gold has been most frequently used in the literature to synthesize high-quality crystalline silicon nanowires,[9] copper catalysts are becoming increasingly common for applications such as solar cells, as they are less detrimental to device performance[10,14] and easier to remove due to copper's high diffusivity.

The chemical driving force for precipitation, μ, for a metal impurity supersaturated in bulk silicon is given by the approximation:[31]

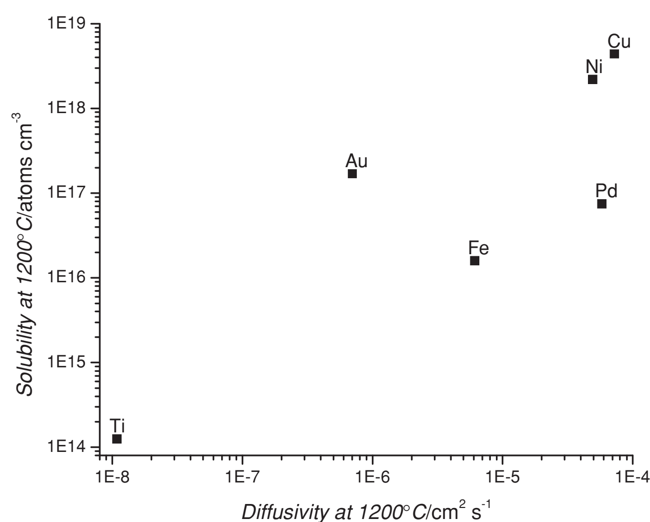

Figure 2. Solubility and diffusivity in silicon of candidate seeding elements at 1200 °C.[29,30] Of all elements assessed above, copper is the most easily manipulated, given its large diffusivity and solubility.

$$\mu = k_B T \times \ln\left[\frac{C}{C_0(T)}\right] \quad (1)$$

where C is the instantaneous concentration of the metal point defects in bulk silicon, $C_0(T)$ is the equilibrium solubility of the metal in silicon as a function of temperature, T, and k_B is the Boltzmann constant. There is a large energy barrier for bulk precipitation of copper, due to the large Cu_3Si/Si interface strain energy, and the energy cost of creating approximately one silicon self-interstitial for every two precipitating Cu atoms.[31] After the initial in-diffusion step, during the rapid quench from high temperature, shown schematically in Figure 1b, μ is large due to the high value of $C/C_0(T)$, and the copper is expected to form a stable silicide of η"-Cu_3Si in the bulk, as has been seen in previous studies.[32,34] However, during the slow cooling after the surface-patterning step shown in Figure 1d, we postulate that the copper has time to diffuse to the surface of the silicon sample and precipitate there, where the energy barrier for nucleation is lower. Additionally, nucleation to a surface defect is generally more energetically favorable than to a smooth surface due to a larger number of facets and/or localized strain. Copper silicide "decoration" around structural defects in multicrystalline silicon has been observed in previous studies.[32]

Figure 3 shows the results of in-diffusing copper at 1200 °C into a <100> silicon sample, patterning pits on the surface with the focussed ion beam (FIB), and the resulting formation of copper squares over the FIB mills. The preferential nucleation of copper on the FIB mills in Figure 3 shows evidence that surface defects such as FIB mills serve as heterogeneous nucleation sites, lowering the energy barrier for precipitation. Increasing the cooling rate could decrease selectivity of surface sites for precipitation. The demonstration of high-throughput seeding on the textured surface of Figure 3 opens up the possibility of seeding on three-dimensional surfaces of even higher aspect ratios.

Figure 4 shows the increase in median precipitate size on the surfaces of smooth, unpatterned silicon <111> wafers

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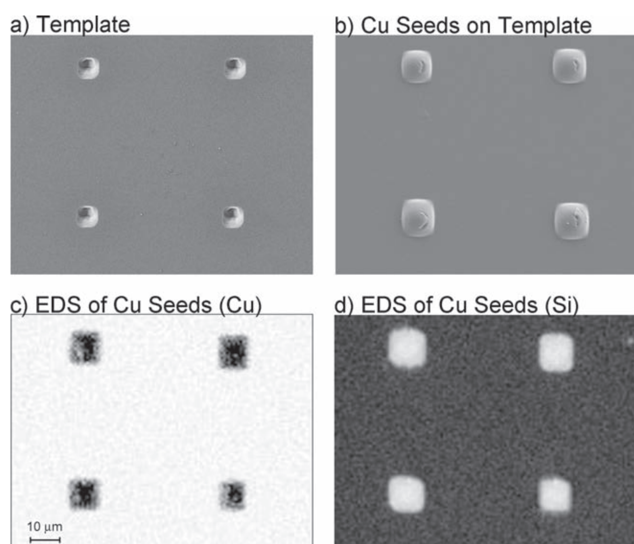

Figure 3. a,b) Surface patterning with FIB demonstrates control over copper seed placement. c,d) Energy dispersive X-ray spectroscopy (EDS) confirms copper content of seeds. (Black represents high counts in EDS maps.)

when the in-diffusion temperature is increased from 1000 to 1200 °C. The size distributions were found by counting the precipitates on the surface with an optical microscope. In Figure 4, we see that by increasing the in-diffusion temperature, we control the size of the copper seed independently of the patterning step. These observations are consistent with the Arrhenius dependence of copper diffusivity and solubility on in-diffusion temperature. We observe triangular particles on silicon <111> wafers as opposed to square precipitates on silicon <100> wafers. The different shapes formed on the <111> and <100> silicon surfaces are consistent with previous studies in which the metals on the surface of silicon self-assembled into shapes along the <110> direction.[35–37]

The size of precipitates could be controlled further by varying the density of favorable nucleation sites (i.e., surface defects), varying the cooling rate (as in Figure 1d), or changing the substrate thickness. With a faster cooling rate and higher density of surface defects, there will be more precipitates of smaller sizes. Increasing the thickness of the silicon substrate allows for more metals to be diffused into the bulk, and thus, larger seed sizes. Other metals, due to differences in solubilities and diffusivities, as shown in Figure 2, can be used to tailor precipitate sizes. Although we demonstrate micron-sized precipitates, we can reduce the wire diameter down to the nanoscale by varying these parameters. Additionally, sacrificial surface defects could be created to act as sinks for metals, possibly on the backside of the wafer, reducing the number of available metal atoms to form seeds, thus offering another degree of freedom to control seed size.

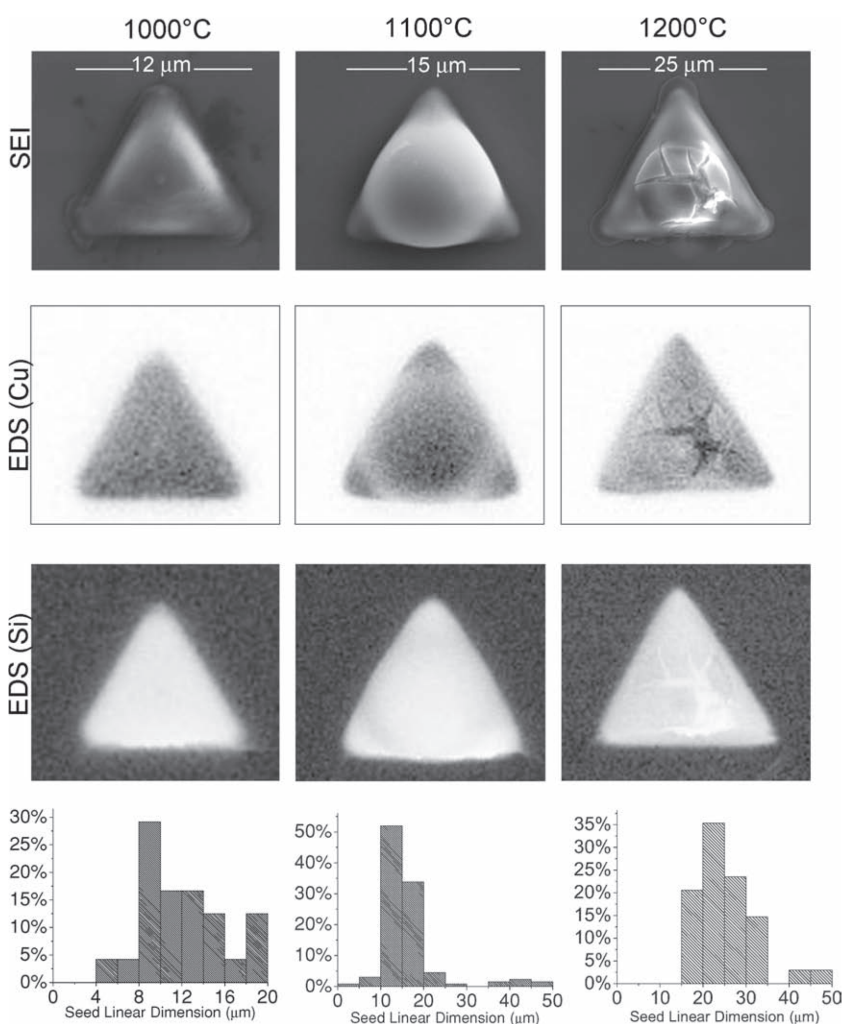

Figure 4. Variation in median copper seed size by changing in-diffusion temperature as shown in secondary electron imaging (SEI). EDS confirms the presence of copper in seeds. (Black represents high counts in EDS maps.)

The precipitates in Figure 3 and Figure 4 have rounded edges; this feature demonstrates that out-diffusion may have occurred by retrograde melting, in which the dissolved metal impurity precipitates into a liquid phase above the metal-silicon eutectic temperature.[38]

Although Figure 3 shows that the positions of metal catalyst seeds with the OMP method can be controlled, FIB milling is low-throughput, and not a practical method of creating surface defects for precipitation in large-scale applications. Higher-throughput methods for creating surface defects, possibly on three-dimensional surfaces, include wet etching, such as stain etching with nitric and hydrofluoric acid[39] or anisotropic etching with potassium hydroxide,[40] mechanical indenting or scratching, reactive ion etching,[41] or laser ablation.[42]

Figure 5 shows a silicon microwire grown from an out-diffused copper seed on a <111> silicon surface. This seed was on a smooth surface with an in-diffusion temperature of 1200 °C. Energy dispersive X-ray spectroscopy (EDS) with scanning

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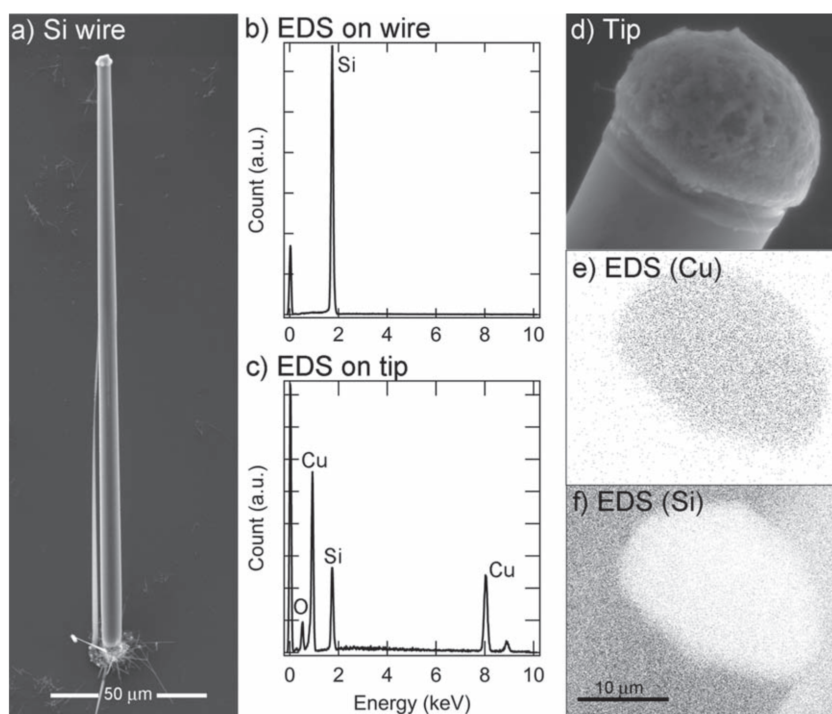

Figure 5. A silicon wire is grown on a copper silicide seed (a), confirmed by an EDS spectrum from a point scan on the wire (b). An EDS spectrum from a point scan taken from the catalyst tip of the silicon wire shows a composition dominated by copper (c). EDS copper (e) and silicon (f) maps of the tip (d) are also shown. (Black represents high counts in EDS maps.)

electron microscopy (SEM) shows that the tip contains copper, and the wire is predominantly silicon. Figure 5 demonstrates that seeds from the OMP method can successfully catalyze VLS growth of silicon wires.

A drawback to the OMP method is substrate contamination with the metal catalyst used. However, with copper's high diffusivity and low solubility at room temperature, combined with a high bulk nucleation energy barrier,[43] bulk contamination levels are expected to be low. It has been shown that lifetime and minority carrier diffusion length are not affected much by low levels of copper impurities in p-type silicon.[44]

The OMP method can also be streamlined. If the amount of metal deposited on the substrate is less than the amount of metal required to saturate the bulk, patterning of the substrate surface can take place before the high-temperature anneal for in-diffusion of the metal, and the slow cool down to room temperature can immediately follow, skipping the need for a rapid quench in silicone oil. For a 600 μm thick sample in-diffused at 1200 °C, the copper layer should be no more than 310 nm thick. Due to the effect of retrograde melting, in which the dissolved metal is forced out of the solid solution in the form of liquid silicon-metal droplets during cool down,[38] there is also a possibility to go from this stage directly to VLS growth of silicon wires.

It is foreseeable that the OMP method could serve to seed catalysts for functional nanoscale devices. Several studies[45–47] attempt direct growth of silicon nanowires in trenches to form transistors. Application of the OMP method in growth of such devices may provide greater control of the distribution of nanowires. Other possible applications include solar cells, such as growth on textured light-capturing surfaces or three-dimensional photovoltaics.[48]

In this communication, we show proof-of-concept for the OMP technique. We demonstrate how to vary the size of these seeds through in-diffusion temperature and how to independently control placement through surface patterning by FIB. By adapting this process to large-area surface-texturing techniques, we believe that the OMP technique has the potential to seed metal catalysts of any size, at any location, on three-dimensional surfaces in a high-throughput manner. We demonstrate OMP with a copper catalyst on silicon, but with understanding of impurity kinetics and knowledge of diffusivity and solubility constants, this technique can be extended to other material systems.

Experimental Section

We use <111> and <100> boron-doped float zone wafers, with resistivities of approximately 20 and 100 ohm cm, and thicknesses of 525 and 675 μm, respectively. The wafers are laser scribed into 1 cm squares and RCA-cleaned. E-beam evaporation is used to deposit 600 nm of Cu on the silicon substrates, enough to completely saturate the silicon at the in-diffusion temperatures used. The sample is then annealed at high temperature for 30 min to in-diffuse copper and rapidly cooled by quenching into silicone oil. Temperatures of 1200, 1100, and 1000 °C are used for the in-diffusion anneal. The annealing time is calculated so that the diffusion length of Cu in Si would be more than 10 times the thickness of the sample, to ensure homogeneity of the metal solute throughout the bulk of the sample. After quenching, the sample is then polished to 0.25 μm roughness on both sides to remove excess metal and ensure a smooth surface. On some samples, surface patterning with a Zeiss NVision 40 Dual Beam Scanning Electron Microscope and Focused Ion Beam (FIB) is performed. A 6.5 nA, 30 keV beam is used to mill squares of 3.5 μm in length and approximately 3 μm deep.

After another RCA-cleaning step, the samples are brought to a temperature 25 °C higher than the in-diffusion temperature, so that we assume the Cu species is completely dissolved in the silicon matrix. Subsequently, the samples are slow-cooled to approximately 300 °C below the in-diffusion temperature at a rate of 2 °C min^{-1}, then cooled to 500 °C at 15 °C min^{-1}. At 500 °C, the samples are removed from the furnace and allowed to cool to room temperature. All furnace anneals took place in a forming gas (93% N_2 and 7% H_2) ambient to prevent surface oxidation.

Silicon wires are grown at the locations of the copper catalyst seeds by atmospheric pressure chemical vapor deposition in a hot wall isothermal reactor tube at 1000 °C. H_2 carrier gas at a flow rate of 15 sccm was bubbled through a vessel containing liquid $SiCl_4$ liquid maintained at a temperature of −11.8 °C. Additional H_2 was added to the inlet stream to maintain a $SiCl_4$ partial pressure

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of 9 Torr during growth. The growth temperature is above the silicon–copper eutectic temperature of 802 °C,[49] which suggests a VLS mechanism of growth.

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